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IAP9 Rec'd PCT/PTO 2 8 AUG 2006

By Express Mail # EV888648196US · August 28, 2006 **Attorney Docket # 5367-257PUS**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re National Phase PCT Application of

Martin KNAIPP

International Appln. No.:

PCT/EP2005/002112

International Filing Date:

February 28, 2005

For:

High-Voltage PMOS Transistor

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

SIR:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56 and in accordance with the practice under 37 C.F.R. §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed Form PTO/SB/08a. Copies of the listed non-U.S. documents are enclosed.

It is respectfully requested that the above information be considered by the Examiner and that the copy of the enclosed Form PTO/SB/08a be returned indicating that such information has been considered.

In accordance with 37 C.F.R §§1.97(g) and (h), the filing of this Information Disclosure Statement should not be construed as a representation that a search has been made or that information cited is, or is considered to be, material to patentability as defined in §1.56(b), or that any cited document listed or attached is (or constitutes) prior art. Unless otherwise

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indicated, the date of publication indicated for an item is taken from the face of the item and Applicant(s) reserve(s) the right to prove that the date of publication is in fact different.

If any fees or charges are deemed required at this time in connection with the application, the same may be charged to our Patent and Trademark Office Deposit Account No. 03-2412.

Respectfully submitted,

COHEN, PONTANI, LIEBERMAN & PAVANE LLP

Thomas Langer

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Dated: August 28, 2006

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Substitute for Form 1449/PTO	Com	plete if Known
	Application Number	
INFORMATION DISCLOSURE	Filing Date	
	First Named Inventor	Martin KNAIPP
STATEMENT BY APPLICANT (Use as many sheets as necessary)	Art Unit	
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Sheet 1 of 1	Attorney Docket Number	5367-257PUS

			U.S. PATE	NT DOCUMENTS	
Examiner Initials*	Cite No. 1	Document Number Number-Kind-Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-6,455,893 B1	09/24/2002	Gehrmann et al.	
		US-			
	-	US-			
		US-			

				TENT DOCUMENTS	1 2 2 1 1	76
Examiner	Cite	Foreign Patent Document	Publication Date	Name of Patentee or	Pages, Columns, Lines,	1
Initials*	No. 1	Country Code ³ Number ⁴ Kind-Code ⁵ (if known	MM-DD-YYYY	Applicant of Cited Document	Where Relevant Passages or Relevant Figures Appear	
		WO 97/13277	04/10/1997	Roth et al.		Abstract
		JP 05-304169	11/16/1993	Hidetashi		Abstract
						only
		JP 05-172220	07/03/1990	Shizunori et al.		Abstract
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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

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Attorney Docket # 5367-257PUS

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Martin KNAIPP

Int'l PCT Serial No.: PCT/EP2005/002112

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28 February 2005

For:

High-Voltage PMOS Transistor

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Submitted herewith is a copy of the International Search Report issued in connection with International Application on which the present U.S. National Phase application is based.

Copies of the references cited in the International Search Report have been supplied by WIPO to the USPTO. Therefore, copies of the cited references in the International Search Report are not being provided herewith in accordance with current U.S. practice because they should be on file already at the USPTO.

It is respectfully requested that the Examiner return an initialed copy of the attached Form PTO SB/08A to confirm that the publications supplied by WIPO and listed therein have been considered and made of record.

Respectfully submitted, COHEN, PONTANI, LIEBERMAN & PAVANE LLP

Ву ___

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Dated: August 28, 2006

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Examiner Initials*	Cite No.	Document Number Number-Kind-Code ^{2 (if}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS								
Examiner	Cite	Foreign Patent Document	Publication Date	Name of Patentee or	Pages, Columns, Lines, Where Relevant	T⁵		
Initials*	No.	Country Code ³⁻ Number ⁴⁻ Kind-Code ^{5 (if known}	MM-DD-YYYY	Applicant of Cited Document	Passages or Relevant Figures Appear			
		EP 0 973 205 A	01/19/2000	Elmos Semiconductor AG				
		WO 03/092078 A	11/06/2003	Sanken Electric Co., Ltd.				
		EP 1 498 956 A	01/19/2005	Sanken Electric Co., Ltd.				
		EP 0 524 030 A	01/20/1993	Fuji Electric Co., Ltd.				
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Sheet	2	of	2	Attorney Docket	5367-257PUS	
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	NON PATENT LITERATURE DOCUMENTS	
Cite No. 1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
	High Voltage Breakdown of Planar Junctions", International Electron	
	Technology", IEEE Electron Device Letters, Vol. 21, No. 1, pp. 40-42,	1.000
	K. Kinoshita et al., "A New Adaptive Resurf Concept for 20 V LDMOS without Breakdown Voltage Degradation at High Current", Proceedings of the 10 th International Symposium on Power Semiconductor Devices and ICS (ISPSD '98), Kyoto, Japan, pp. 65-68, June 3, 1998	
		Cite No. Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. R. Stengl et al., "Variation of Lateral Doping - A New Concept to Avoid High Voltage Breakdown of Planar Junctions", International Electron Devices Meeting, Washington, D.C. USA, pp. 154-157, December 1, 1985 C. Bassin et al., "High-Voltage Devices for 0.5-MUM Standard CMOS Technology", IEEE Electron Device Letters, Vol. 21, No. 1, pp. 40-42, January 2000 K. Kinoshita et al., "A New Adaptive Resurf Concept for 20 V LDMOS without Breakdown Voltage Degradation at High Current", Proceedings of the 10 th International Symposium on Power Semiconductor Devices and

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